DESIGN, SIMULATION AND IMPLEMENTATION OF ASYMMETRIC DIGITAL SUBSCRIBER LINE MODEM ON DSP KIT

HOSSAM LABIB A. ZAYED
Higher Institute of Technology-
Benha University, Benha, Egypt

A.A.ZEKRY
Faculty of Engineering-Ain Shams
University, Cairo, Egypt

ADEL EZAT ELHENNAWY
Faculty of Engineering-Ain Shams
University, Cairo, Egypt

AYMEN MOSTAFA HASSAN
Higher Institute of Technology-
Benha University, Benha, Egypt

ABSTRACT
In this paper, design, simulation and implementation of Asymmetric Digital Subscriber Line (ADSL) modem is presented which can be applied to different telephone networks. The ADSL modem is modeled and simulated under the MATLAB version 7.3 (R2006b) environments by which the simulation is achieved for both the downstream and upstream directions of the modem. The ADSL modem with a transmission throughput between 640 kbps and 6 Mbps operating over most of existing telephone subscriber loops has been implemented on TI TMS320C6713 DSP for consumer multimedia applications. Except the Analog Front End, all the basic building blocks of the ADSL modem functionalities are implemented with DSP platform. We use Real-Time Data Exchange (RTDX) as a way to debug and test our DSP designs.

INTRODUCTION

Asymmetric Digital Subscriber Line (ADSL) is a high speed data transmission technology that allows reuse of existing copper phone line [1]. It allows up to 8 Mbps data transmission on downstream and 640 Kbps on upstream[2]. To increase the spectral efficiency of the available bandwidth, ADSL employs a transmission technique based on Multicarrier modulation, namely, discrete multitone (DMT) [3, 4]. ADSL uses two separate frequency bands, the band from 25.875 kHz - 138 kHz is used for upstream communication, while 138 kHz – 1104 kHz is used for downstream communication.

DMT divides the available bandwidth into N parallel subchannels or tones, by means of an N-point inverse fast Fourier transform (IFFT). At the transmitter, each tone is modulated by quadrature amplitude modulation (QAM) and IFFT transformed to obtain a time domain signal. At the receiver, an N-point FFT can be used for demodulation. Prepending each data block after IFFT modulation with a cyclic prefix ensures that the subchannels remain independent after transmission over a channel. If the order of the channel is smaller than the cyclic prefix length, ν, the transmitted signal can easily be recovered by the so-called frequency domain equalizers (FEQs). Besides equalization, echo cancellation is required to separate upstream and downstream signals and to enable efficient bidirectional communication over the same telephone wire. Echo cancellation can improve the reach and/or noise margin of an ADSL system by allowing both

upstream and downstream signals to share the low frequency portion of the available frequency band.

Daniel [5], proposed and implemented a new link aggregation model for ADSL that operates with any combination of circuit rates, supports dynamic link rate changes, and requires minimal overhead. He implemented his model using standard ADSL equipment and provided a data rate of 20Mbps at 13,500 feet using four ADSL circuits with very low latency and jitter. Liang [6], presented a modified method based on multi-user detection, which can mitigate the crosstalk interference in DMT-ADSL receiver. Miloš [7], proposed an equalizer design that maximizes the bit rate of a DMT system at the output of the FFT demodulator and introduced a novel receiver architecture that uses time domain per-tone equalizer filter bank (TEQFB) that maximizes a measure of the ADSL system bit rate. Ravishankar [8], proposed a new bit-loading algorithm that reduces the power required to transmit data. He simulated and implemented such ADSL system with bit- loading algorithm. Ming [9], introduced a linear phase Time Domain Equalizer (TEQ) that exploits symmetry in existing eigen-filter approaches such as minimum intersymbol interference (Min-ISI) equalizers. Sobia [10], discussed the use of discrete multitone technology at the PHY layer of an in-home power line communication network, particularly with reference to bit-loading techniques.

In this paper, ADSL system is presented and simulated under the MATLAB version 7.3 (R2006b) environments to test the system performance. The proposed system is implemented on TI TMS320C6713 DSP kit. All the basic building blocks of the ADSL modem functionalities are implemented, tested and debugged using Real-Time Data Exchange (RTDX).

ADSL MODEM SIMULATION

Both the downstream and upstream paths that represent the ADSL modem are simulated and tested under different amount of noise using MATLAB version 7.3 (R2006b) environments. Asymmetric data rate is achieved by taking different bandwidth for FFT/IFFT pair in each direction. The design parameters that are used in the simulation are summarized in Table1.

In the ADSL modem simulation, no pilot carriers are used since no synchronization problem is considered and perfect knowledge of the channel transfer function is assumed at the receiver for simplification purposes. Figure1 shows the overall block diagram for the ADSL transmitter and receiver.

Parameter	Downstream	Upstream
Number of subchannels	256	32
FFT/IFFF size	512 points	64 points
Cyclic Prefix Length	32 samples	4 samples
Nyquist Frequency	1.104 MHz	138 KHz
Sampling Frequency	2.208 MHz	276 KHz
Subchannel BW	4.3125 KHz	4.3125 KHz
Symbol Time	250 µSecond	250 µSecond

Table 1 ADSL Simulation Parameters

As shown in Figure 1, the binary input data are separated into two parallel paths, the first one (the path at the top of the figure) is called the fast path or the

fast buffer, while the other is the interleaved path or buffer. The interleaved path supports a convolutionally interleaved RS error correction. Interleaving operation increases the second path resistance to burst errors, but also it increases its latency. The greater resistance to errors in the interleaved path is meant to support applications that are sensitive to degradation due to errors induced by line noise but relatively tolerant to increased latency. Moreover, the data in the second path is modulated to the high frequencies subcarriers by which they are vulnerable for attenuation in such high frequencies. The fast path provides less protection against transmission errors but less delay. It is meant to transport delay-sensitive applications such as interactive data.

The sequence of the coding techniques appeared in Figure 1 is arranged as follows: At the beginning, the CRC bits are added in order to flag error detected at the end of the reception, thus detecting errors that are not corrected by the RS code. After the CRC, the scrambler scrambles the data sequence so that problems come with the long string of 0s and 1s are reduced and avoided. After that, the RS code appends certain bits for data correction and attempt to correct the received bits with errors. Finally, the interleaver in the interleaved path has a significant role to reduce burst errors and make the errors within the RS code correctable number of errors.

After the error detection and correction codes as well as scrambling and interleaving, the data are modulated using the DMT modulator, by which the input stream is divided into 256 subchannels in accordance with the 256 carriers of the ADSL specifications for the downstream path, and 32 subchannels for the upstream path. The output signal from the DMT modulator is totally real, because the real part of frequency domain signal has an even symmetry and the imaginary part which in turn has an odd symmetry, and this is due to Hermitian symmetry.

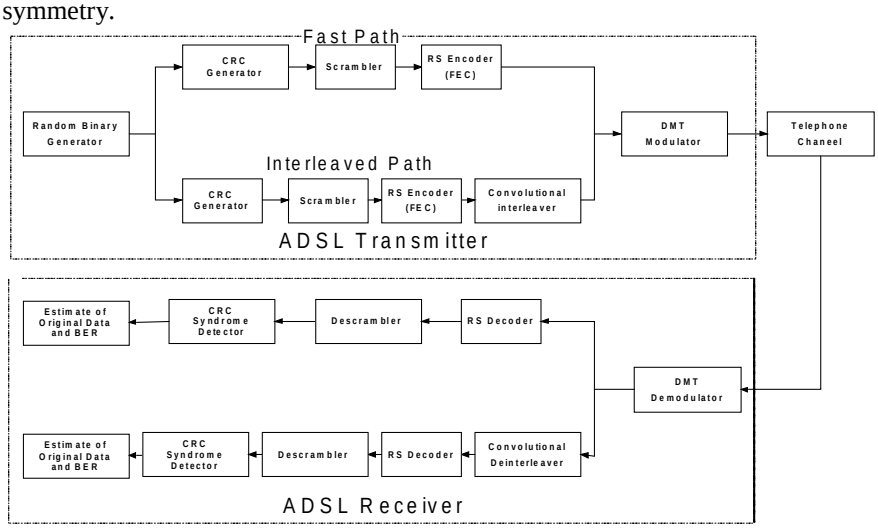

Figure 1. The Functional ADSL Modem Simulation Model.

ADSL TRANSMITTER

The transmitter consists of the following functional blocks.

1. INPUT DATA SOURCE

The data source is modeled as Bernoulli Binary Generator block that generates random binary numbers with equal probability of zeros and ones. The output data is a frame-based matrix and frame rate is 4000 frame/sec. For the downstream path, the number of bits per frame is equal to 1552 and the sample time is 0.16108 µSecond with one sample/bit. For the upstream path, the number of bits per frame is equal to 92 and the sample time is 2.71739 µSecond with one sample/bit.

The transmitter contains two parallel paths. One path (the fast buffer) processes the first 776 bits of each 1552-bit data frame, while the other path (the interleaved buffer) processes the last 776 bits of each data frame. In case of upstream path the fast buffer processes the first 46 bits and the interleaved buffer processes the last 46 bits of each data frame.

2. GENERAL CRC GENERATOR

Cyclic redundancy check (CRC) coding is an error-control coding technique for detecting errors that occur when a message is transmitted. When an error is detected in a received message word, the receiver requests the sender to retransmit the message word. In CRC coding, the transmitter applies a rule to each message word to create extra bits, called the checksum, or syndrome, and then appends the checksum to the message word. After receiving a transmitted word, the receiver applies the same rule to the received word. If the resulting checksum is nonzero, an error has occurred, and the transmitter should resend the message word.

The General CRC Generator block generates cyclic redundancy code (CRC) bits for each input data frame and appends them to the frame. Each path (fast or interleaved) appends eight cyclic redundancy check (CRC) bits to its 776-bit frame.The uesd generator polynomial is $G(D) = D^8+D^4+D^3+D^2+1$ (1)

3. THE SCRAMBLER

The bit stream from the CRC generator is then passed through a self-synchronizing scrambler to break up long strings of 1's and 0's. The connection polynomial is $P(z^{-1})=1+z^{-18}+z^{-23}$ (2)
with zeros for the Initial states of the linear feedback shift registers.The scrambling and encoding operations interpret the bits as integers between 0 and 127. The inputs to scrambler are serial bits so we use Bit to Integer Converter block .The Bit to Integer Converter block maps groups of bits in the input vector to integers in the output vector. The Number of bits per integer parameter is 7, and then the block maps each group of 7 bits to an integer between 0 and 127.The scrambler and FEC (RS Encoder) block is shown in Figure 2.

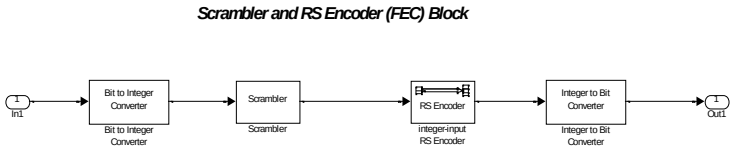

Figure 2. The Scrambler and RS Encoder.

4. REED-SOLOMON (RS) ENCODER

Successive blocks of bits from the scrambler are operated on by the Reed-Solomon encoder which adds redundant bits to the blocks so that transmission errors can be corrected at the receiver. This process is often called forward error correction (FEC). RS codes are used in DSL because they provide coding gain against random errors (of about 3dB) [1]. RS code is a systematic linear block code. Each block is further subdivided into M-bit symbols. An RS code is specified as RS (N, K) with M-bit symbols.

The Integer-Input RS Encoder block creates a Reed-Solomon code with message length K and codeword length N. An (N, K) Reed-Solomon code can correct up to floor ((N-K)/2) symbol errors (not bit errors) in each codeword. The input and output are integer-valued signals that represent messages and codewords, respectively. The input must be a frame-based column vector whose length is an integer multiple of K. The output is a frame-based column vector whose length is the same integer multiple of N, and whose data type is inherited from the input [11].

RS code is based on a finite field called the Galois Field (GF). For the ADSL modem design, all arithmetic in the RS codes are byte-wise in the finite field GF256 ($GF(2^8)$), that means every symbol in an RS code for ADSL is a byte (8 bits).

In our block we used RS (120,112) code with error correcting capability of 4 bytes/symbol. In case of upstream path we used RS (15, 9) code with error correcting capability of 3 bytes/symbol.

5. CONVOLUTIONAL INTERLEAVER

In the second path a convolution interleaver block interleaves the encoding data. This interleaving operation increases the second path resistance to burst errors but also its latency.

An impulse noise can corrupt several multi-carrier symbols and cause bursts of errors in the received data streams if no special precautions are taken. ADSL systems protect against bursts in two ways. First, the Reed-Solomon codes discussed in the previous section naturally can correct multiple bit errors in a single code symbol, which consist of a string of eight bits, since any pattern of eight or less bits is treated as a single code symbol error. Second, a technique

called interleaving is required by the standards for the data streams needing low error rates [12].

In the simulated ADSL modem, a convolutional interleaver is used. The Convolutional Interleaver block permutes the symbols in the input signal. Internally, it uses a set of shift registers. The delay value of the kth shift register is (k-1) times the Register length step parameter. The number of shift registers is the value of the Rows of shift registers parameter.

For both the downstream and upstream paths, the interleaving depth that is used in the simulation is equal to 2 and the number of shift registers is equal to 5. So this causes a delay equal to 40 samples.

The data from the two paths (fast and interleaved) is concatenated to create contiguous output signal.

6. DISCRET MULTITONE (DMT) MODULATOR

The DMT block diagram that is used in the ADSL modem simulation is shown in Figure 3. The DMT signaling technique divides the channel into 256 subchannels and modulates each one individually. Each of the 16 Modulator Bank icons represents a set of 16 Rectangular QAM Modulator Baseband blocks The DMT technique allocates different numbers of bits to different subchannels. Each copy of the modulator block acts as a distinct subchannel, and uses the 256-element bit allocations to determine the M-ary number parameter that is appropriate for that subchannel. The system has 256 modulator blocks in total in case of downstream path and 32 modulator blocks in total in case of upstream path.

After concatenating the coded data bits, these bits are then assigned to each of the N/2 = 256 subchannels using a bit loading algorithm called water-filling algorithm [13,14]. In the simulated modem, a specific bit loading distribution is used by which the number of bits/subchannel is varied from 1 up to 12 bits. The second step in DMT modulation is the mapping of the assigned bits to subsymbols using variable-size QAM constellation. QAM is used to map the input bit stream into complex values in frequency domain samples. To obtain time domain real samples we use IFFT. The array of (N/2)=256 complex values with their conjugate symmetric one should enter the IFFT block to generate N=512 real time domain samples. The obtained time domain samples are called a DMT symbol . For the downstream path of the presented modem, the IFFT size is 512 point, and for the upstream path, 64 point IFFT is used.

Each DMT symbol is prepended by (1/16) of the symbol itself called cyclic prefix to eliminat Intersymbol Interference (ISI). After the FFT in the receiver, the subsymbols are the product of the N-point FFT of the channel impulse response and the N-point FFT of the transmitted subsymbols [15]. For the downstream path of the ADSL modem, CP is realized by copying the last 32 samples from the 512 samples of the DMT symbol and appending them to the beginning of this DMT symbol. And for the upstream path, the last 4 samples are copied and appended to the beginning of the DMT symbol that consists from 64 samples.

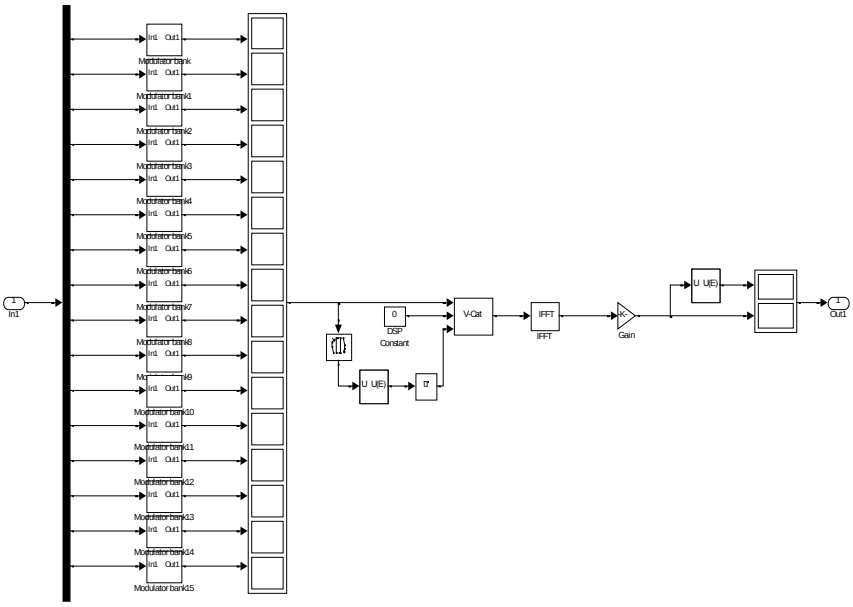

Figure 3. DMT Modulator.

THE TELEPHONE CHANNEL

The telephone line is modeled as a Finite Impulse Response (FIR) filter of length 101 and the Additive White Gaussian Noise (AWGN) channel as a source of the noise. For simplicity, the modeled channel that is used in the ADSL system is considered as an equalized channel, i.e. its impulse response is assumed to be equalized by a TEQ. The frequancy and phase response of the channel are shown in figure 4,5 respectively.

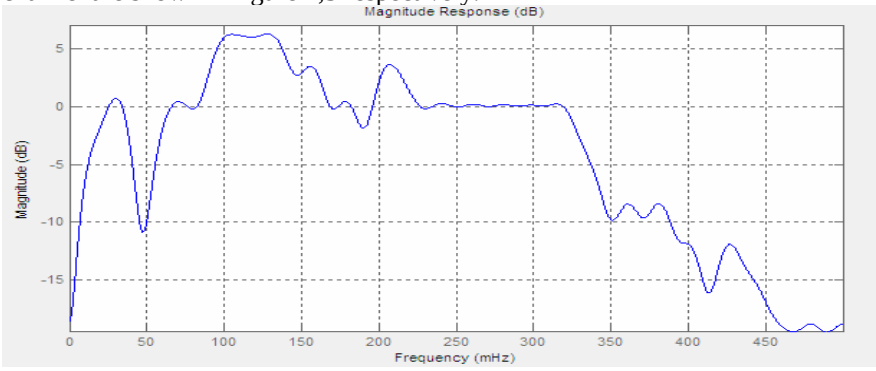

Figure 4. The Frequency Response of the Channel.

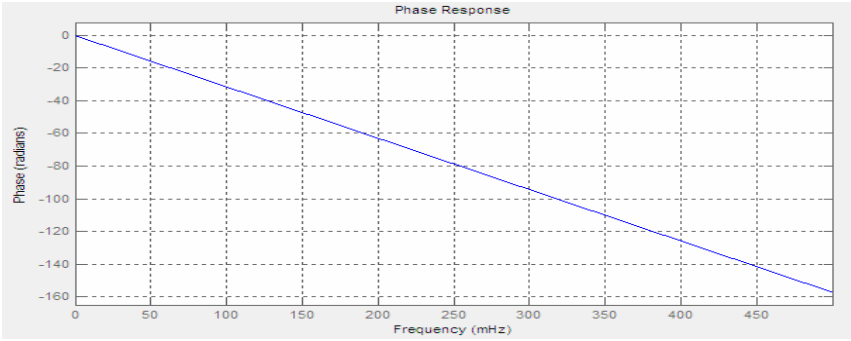

Figure 5. The Phase Response of the Channel.

ADSL RECEIVER

The receiver attempts to undo each operation that the transmitter performs and eventually generates the original data bit stream after demodulation and decoding processes. For example, to undo the actions of the Convolutional Interleaver block, use a Convolutional Deinterleaver block with the same mask parameters.

SIMULATION RESULTS

The frequency spectrum for the transmitted data at the transmitter side of the downstream path and the upstream path of the ADSL modem are plotted as shown in figure 6, 7 respectively.

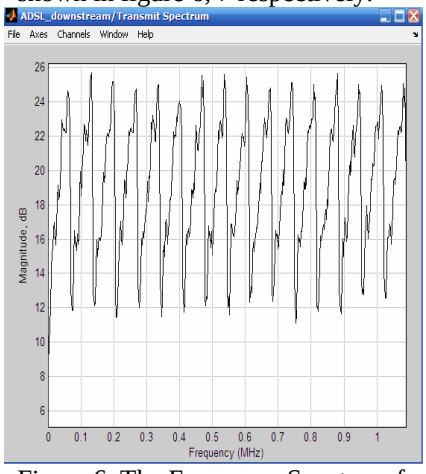

Figure 6. The Frequency Spectrum for Transmitted data at Downstream path

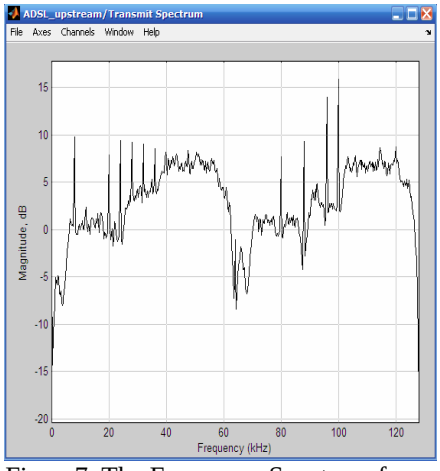

Figure7. The Frequency Spectrum for Transmitted data at Upstream path

HARDWARE IMPLEMENTATION

The C6713 is considered to be one of the Texas Instruments™ most powerful processors; but it's practical application are greatly minimized if it is not made to operate in the standalone state [16], the CPU is based on very long instruction word (VLWI) architecture. This processor has eight functional units that works in parallel, six arithmetic logic units (ALUs) and two multiplier units with whom a total of eight 32-bit instructions can be fetched every clock cycles, also it contains 264 kB of internal memory and two sets of 32-bit general purpose registers. The CPU operates at 225MHz delivering a peak performance of 1.35 giga-floating-point operations per second (GFLOPS) and 450 million multiply accumulate cycles per second (MMACS)[17,18,19]. The DSK connects to a host PC via a USB port. The TMS320C6713 DSK board includes:

- 32- bit stereo codec TLV320AIC23 with two inputs and two outputs , variable sampling rates from 8 to 96 KHz.
- 16 MB of synchronous dynamic random access memory (SDRAM).
- 256 kB of flash memory.
- Four light-emitting diodes (LEDs) and four dip switches.
- External memory interface (EMIF).

Finally it comes with a powerful PC software in the form of Code Composer Studio (CCS) is provided in order to enable software written in C or assembly language to be compiled and/or assembled, linked, and downloaded to run on the DSK [20].

The Embedded Target for TI C6000 DSP provides the Application Programming Interface (APIs) required by real time workshop to generate a code specifically for the C6000 platform. MATLAB Simulink uses a block based approach implementation instead of complex algorithm design. Link for Code Composer Studio is used to invoke the code building process. This code can then be downloaded on the target from where it runs. The data on the target is accessible in CCS or in MATLAB via link for CCS or via Real-Time Data Exchange (RTDX).

Link for RTDX Interface provides a communications pathway between MATLAB and digital signal processors installed on the PC. Using objects in the MATLAB Link for Code Composer Studio, you open channels to processors on boards in your computer and send and retrieve data about the processors and executing applications, as well as send data to the processes for use and get data from the applications.

The general structure of the implemented ADSL transmitter and receiver system is depicted in Figure 1. We added some blocks to the ADSL system model to be implemented on the DSP kit. The added blocks are shown in Figure 8. The system level design was made using Matlab version 7.3 and Code Composer Studio 3.1. The implementation is done through cooperation for direct code generation from the MATLAB and execution at the TMS320C6713 DSK development kit using CCS3.1. The output of the transmitter and receiver (non-interleaved path and interleaved path) are taked and displayed by four RTDX output channels named Tx_Non_Int_out, Rx_Non_Int_out, Tx_Int_out and Rx_Int_out respectively. The RTDX output channels for non-interleaved path and interleaved path are shown in figure 9. As shown in figure 9 the output data bits of the received channel Rx_Non_Int_out is the same as the transmitted channel Tx_Non_Int_out but in the case of interleaved path there are 7 bits

delay between the received channel Rx_Int_out and the transmitted channel Tx_Int_out. The corresponding delay is due to latency of the interleaved path.

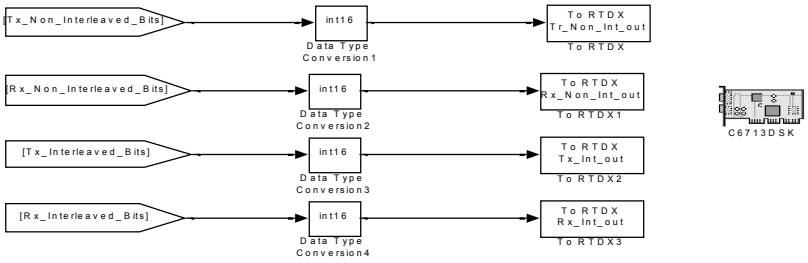

Figure 8. The Added Blocks to the ADSL System Model

Data

	Tx_Non_Int_	Rx_Non_Int_	Tx_Int_out	Rx_Int_out
1	0	0	0	0
2	0	0	0	1
3	0	0	1	1
4	1	1	1	0
5	1	1	1	0
6	1	1	1	1
7	1	1	0	0
8	0	0	1	0
9	1	1	0	0
10	0	0	1	1
11	1	1	1	1
12	1	1	0	1
13	0	0	0	1
14	0	0	1	0
15	1	1	0	1
16	0	0	0	0
17	0	0	0	1
18	0	0	1	1
19	1	1	1	0
20	1	1	1	0
21	1	1	1	1
22	1	1	0	0
23	0	0	1	0
24	1	1	0	0
25	0	0	1	1
26	1	1	1	1
27	1	1	0	1
28	0	0	0	1
29	0	0	1	0
30	1	1	0	1
31	0	0	0	0
32	0	0	0	1
33	0	0	1	1
34	1	1	1	0
35	1	1	1	0
36	1	1	1	1

Figure 9. The Four RTDX Output Channels of the Transmitter and Receiver

CONCLUSIONS

In this work, both the downstream and upstream directions of the ADSL modem were modeled and simulated using MATLAB as well as implemented in a DSP platform using the C6713 floating point DSP. All the basic building blocks of the ADSL modem functionalities were implemented, tested and debugged using RTDX. A complete agreement between the transmitted and received data was obtained indicating the success of the implementation.

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